

"1 0 0 1"

"1 0 0 0"

"1 1 1 1"

"1 1 1 0"

"1 1 0 1"

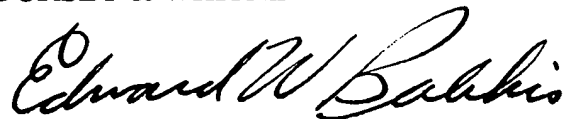
"1 1 0 0"

Again ignoring the LSB, it can be seen that the above sequence consists of a decrementing count in which the bits toggle correctly for an interleave sequence as explained above, and that the column address for each pair of addresses is the same for both the even and the odd addresses in each pair.

REMARKS

Attached hereto is a marked-up version of the changes made to the specification by the current amendment. The attached page is captioned "Version with Markings to Show Changes Made".

Respectfully submitted,
DORSEY & WHITNEY LLP



Edward W. Bulchis
Registration No. 26,847

EWB:dms

Enclosures:

Postcard

Fee Transmittal Sheet (+ copy)

Copy of Notice to File Corrected Application Papers

1420 Fifth Avenue, Suite 3400
Seattle, WA 98101-4010
(206) 903-8800 (telephone)
(206) 903-8820 (fax)

h:\ip\documents\clients\micron technology\700\500794.01\500794.01 supp prelim amnd.doc